REMARKS

In the Official Action, all pending claims 1-17 were rejected by the Examiner. Reconsideration of the application in view of the remarks set forth below is respectfully requested.

Objection to the Specification

In the Official Action, the Examiner objected to the title of the invention as being "not descriptive." Applicants have amended the title of the invention to "Coherency Control Module for Maintaining Cache Coherency in a Multi-Processor-Bus System," which is believed to be descriptive of the Applicants' invention. Accordingly, withdrawal of the objection to the title is respectfully requested.

First Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 1-4, 8-12, 16 and 17 under 35 U.S.C. § 103(a) as being unpatentable over Donley et al. (U.S Patent No. 5,822,611) in view of Merchant (U.S Patent No. 5,893,151). Specifically, with regard to independent claims 1 and 10, the Examiner stated:

> As per claims 1, 10 and 11, Donley discloses a computer system (fig. 1) comprising: a host controller (e.g. cache controller); a first processor bus (local processor bus) coupled between the host controller (cache controller) and a first processor (local processor); a second processor bus (e.g. bus 50) coupled between the host controller (cache controller) and a second processor (processor (processor(s) 1-a', 1-a"); a random access memory (1-M) coupled to the host controller via a memory bus (fig. 1), the RAM comprising a portion of static memory and a portion of dynamic memory; and a static RAM interface module configured to access an address look-up table corresponding to data stored in the static portion of the RAM (tag look-ups; col. 2, lines 1-23); and a coherency control (1-acc) module operably coupled to the first processor bus and the second processor bus and comprising: a request module

> configured to receive requests from the first processor bus and the second processor bus and to maintain proper ordering of the requests from each processor bus (e.g. col. 1, lines 63 et. seq. bridging col. 2, lines 1-50). Donley also discloses requests ordering method, which uses cycle ID (col. 4, lines 15-27). However, Donley does not explicitly teach "an active snoop queue (ASQ) module coupled to the request module and configured to maintain a list of requests currently being processed and to prevent simultaneous multiple accesses to a single address in the static portion of the RAM."
>
> Merchant, in his system for maintaining cache coherency in a multiprocessor environment, teaches a snoop queue 408 is used to maintain a list of requests currently being processed and to prevent simultaneous multiple accesses to a single address in the cache (Abstract; see also fig. 4, col. 8, lines 9-67).
>
> It would have been obvious to one or ordinary skill in the art to modify the coherency control of the Donley system to include the snoop queue module as taught by Merchant, in that Merchant states that such modification would allow ordering of requests to be properly tracked and resolve multiple conflicting snoop requests thus enhancing the overall performance of the system which depends upon the ability to share data in a coherent manner (col. 2, lines 1-20).
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> Official Action, pages 3-4.

Applicants respectfully traverse this rejection. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected

combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

The present application is directed to a technique for filtering processor cache snoops in a multi-processor-bus system. Because each of the processors in a multi-processor system may have separate caches that share a common memory, it is desirable to keep the caches in a state of coherency by ensuring that any shared operand is changed in any cache throughout the entire system. *See id.* at page 5, line 24 to page 6, line 5. Accordingly, processors may snoop a bus to determine if the bus has a copy of the block of data, such that the most current data may be obtained. *See id.* at page 6, lines 4-14. Maintenance of cache coherency is further complicated when a computer system includes multiple processor buses. *See id.* at page 6, lines 16-18. In accordance with the present application, a mechanism is provided to efficiently facilitate snooping of all of the buses in a multi-processor/ multi-bus system to maintain cache coherency. *See id.* at page 10, lines 2-4. In accordance with one embodiment of a multi-processor-bus system, a host controller 16 may be coupled to processors 12A-12D via a first bus 14A, processors 12E-12H via a second bus 14B, and memory controllers 20A-20E via buses 22A-22E. *See id.* at Fig. 1; page 8, line 8 to page 9, line 12. Because the split bus configuration complicates coherency, a cache coherency module is disclosed to provide a centralized management mechanism that efficiently facilitates snooping of the buses in a multi-processor/multi-bus system. *See id.* at page 9, line 22-page 10, line 4. In accordance with one embodiment, a tag control (TCON) module 40, which includes different functional blocks, is provided to manage the snooping process. *See id.* at page 10, lines 15-19. The

(TCON) module may reside in the host controller or, may reside in another device having access to each of the buses but existing independent of the host controller. *See id.* at page 10, lines 19-21.

This multi-processor-bus system is clearly recited in each of the independent claims 1 and 10. Specifically, independent claim 1 recites "a first processor bus coupled between the host controller and a first processor," "a second processor bus coupled between the host controller and a second processor," "a random access memory (RAM) coupled to the host controller via a memory bus, the RAM comprising a portion of static memory and a portion of dynamic memory" and "an active snoop queue (ASQ) module coupled to the request module and configured to maintain a list of requests currently being processed and to prevent simultaneous multiple accesses to a single address in the static portion of the RAM." Further, independent claim 10 recites "a request module configured to receive requests from a plurality of buses" and "an active snoop queue (ASQ) module coupled to the request module and configured to maintain a list of requests from all of the buses currently being processed and to prevent multiple accesses to a single address in the cache memory simultaneously." As such, each of the independent claims recites a centralized management mechanism for efficiently facilitating snooping of buses in the multi-processor/multi-bus system.

In contrast to the claimed subject matter, the Donley reference does not show a multi-processor/multi-bus system. In the Donley reference, processor/cache modules 1-a, 1-a', and 1-a'' are coupled to a main memory 1-M and IO bus bridge 1-B via a system bus 50. *See* Donley, Fig. 1, col. 1, lines 49-56. The processor/cache module 1-a includes a local processor 1a-P having a local cache controller 1-acc and local cache memory 1-ac coupled

through a local processor bus 1-b'. *See* Donley, col. 1, lines 57-67. As such, the Donley reference shows a *single* multi-processor system bus configuration, not a multi-processor/multi-bus system.

The Merchant reference also shows a single multi-processor system bus configuration, not a multi-processor/multi-bus system. The Merchant reference describes a system for maintaining cache coherency by utilizing a snoop queue to block snoopable requests until a blocking condition is satisfied. *See* Merchant, col. 2, lines 23-29. In Merchant, microprocessors 2, 4, 6 and 8 are coupled to a memory controller 12 and I/O bridge 10 via a system bus 20. *See* Donley, Fig. 1; col. 3, lines 24-33. A snoop queue 408 is internal to the microprocessor 2 and acts as an interface for the L1 and L2 caches. *See id.* at Fig. 4; col. 8, lines 22-31. As such, the Merchant system merely describes utilizing a snoop queue that is internal to a microprocessor of a *single* system bus configuration.

In the rejection, the Examiner asserted that the Donley reference disclosed all of the recited features, but does not explicitly teach "an active snoop queue (ASQ) module coupled to the request module and configured to maintain a list of requests currently being processed and to prevent simultaneous multiple accesses to a single address in the static portion of the RAM." In an attempt to cure the deficiencies of the Donley reference, the Examiner relied on the Merchant reference. Accordingly, the Examiner asserted that various structures of the Donley and Merchant references were equivalent to features of the claims. For instance, the Examiner asserted that a local processor bus 1-b'of Donley is equivalent to the "first processor bus" of the claim and a system bus 50 of Donley is equivalent to "the second processor bus" of the claims. The Examiner further asserted that the local cache memory 1-ac is equivalent to the "random access memory" of the claims, and the local cache controller 1-

acc of Donley is equivalent to each of the "host controller" and the "coherency control module" of the claims. However, despite the Examiner's foregoing assertions, the Donley and Merchant references fail to disclose all the claimed subject matter, as discussed below.

First, the Examiner appears to have erroneously construed the Donley reference in relation to the features of the presently recited claims. For example, the Examiner asserted that the local cache controller 1-acc is equivalent to each of the "host controller" and the "coherency control module" of the claims. While the coherency control module *may* be a part of the host controller, the coherency control module may also be a separate element from the host controller, as described in the present application. *See* Application, page 10, lines 15-21. Claim 1 recites a "host controller" and a "coherency control module." By characterizing the local cache controller 1-acc of the Donley reference as both the recited host controller *and* the recited coherency control module, the Examiner has read limitations into the claims that are not supported because the recited features may be separate. Further, the Examiner asserted that the local processor bus 1-b' is equivalent to the "first processor bus" and appears to assert that it is also equivalent to the "memory bus" of the claims. Again, these features are described as separate elements in the present application. *See* Application, Fig. 1; page 8, line 8 to page 9, line 12. As such, the Examiner has erroneously construed the Donley reference as it is applied to certain features of the present claims. For these reasons alone, it should be clear that the present rejections are insufficient to support a *prima facie* case of obviousness.

Secondly, the Donley and Merchant references fail to disclose or suggest "a first processor bus coupled between the host controller and a first processor" and "a second processor bus coupled between the host controller and a second processor," as recited in claim 1, and "a plurality of buses," as recited in claim 10 and having the limiting features

relating to those elements. Specifically, the Donley reference discloses a single system bus 50 coupled to processor/cache module 1-a, 1-a', and 1-a''. *See* Donley, Fig. 1; col. 12, lines 49-56. As noted above, the processor/cache module 1-a includes a local processor bus 1-b', which the Examiner asserted was equivalent to the "first processor bus." *See* Donley, col. 1, lines 57-67. This assertion by the Examiner is not a reasonable interpretation of the present claims. As noted above, Applicants clearly describe and illustrate multiple processor buses, such as bus 14A and 14B, which are the "first processor bus" and the "second processor bus." *See* Application, Fig. 1; page 6, lines 16-24; page 8, lines 8-18. Accordingly, the *processor bus* of the present application is equivalent to the system bus 50 of the Donley reference. As such, one of ordinary skill in the art would not reasonably interpret the local processor bus 1-b', which is simply an *internal* bus to the processor/cache module 1-a, to be equivalent to either the "first processor bus" or the "second processor bus" of the present claims. Thus, the Donley reference fails to disclose or suggest multiple processor buses.

Furthermore, while the Examiner did not rely upon the Merchant reference to disclose the claimed subject matter, the Merchant reference fails to cure this deficiency of the Donley reference. As discussed above, the Merchant reference simply describes a single system bus 20 coupled to the microprocessors 2, 4, 6, and 8. Again, this single system bus configuration cannot be reasonably correlated with the "first processor bus" and the "second processor bus," as recited in claim 1, or "a plurality of buses," as recited in claim 10. Because the Merchant reference fails to disclose this claimed subject matter, it fails to cure the deficiencies of the Donley reference. Thus, the cited references, taken alone or in combination, fail to disclose this claimed subject matter.

Thirdly, the Donley and Merchant references fail to disclose or suggest "a random access memory (RAM) coupled to the host controller via a memory bus, the RAM comprising a portion of static memory and a portion of dynamic memory," as recited in claim 1. As noted above, the Examiner asserted that the local cache memory 1-ac is equivalent to the "random access memory" of the claim 1. However, in the Donley reference, the local cache memory 1-ac is devoid of any mention of a portion of static random access memory or dynamic random access memory. The reference only mentions tag RAM, which is typically a bank of static random access memory used to store addresses. As such, the Donley reference does not disclose "a random access memory (RAM) coupled to the host controller via a memory bus, the RAM comprising a portion of static memory and a portion of dynamic memory," as recited in claim 1.

Furthermore, while the Examiner did not rely upon the Merchant reference to disclose this claimed subject matter, the Merchant reference fails to cure this deficiency of the Donley reference either. As discussed above, the Merchant reference simply describes a single system bus 20 coupled to the microprocessors 2, 4, 6, and 8. Again, the Merchant system is a single system bus configuration and does not disclose a "host controller," much less, "a random access memory (RAM) coupled to the host controller via a memory bus, the RAM comprising a portion of static memory and a portion of dynamic memory," as recited in claim 1. Because the Merchant reference to disclose this claimed subject matter, it fails to cure the deficiencies of the Donley reference. As such, the cited references, alone or in combination, fail to disclose the claimed subject matter.

Finally, the Donley and Merchant references fail to disclose or suggest a coherency control module coupled to multiple processor buses and comprising "an active snoop queue

(ASQ) module coupled to the request module and configured to maintain a list of requests currently being processed and to prevent simultaneous multiple accesses to a single address in the static portion of the RAM," as recited in claim 1, or a coherency control module coupled to multiple processor buses and comprising "an active snoop queue (ASQ) module coupled to the request module and configured to maintain a list of requests from all of the buses currently being processed and to prevent multiple accesses to a single address in the cache memory simultaneously," as recited in claim 10. As noted above, the Examiner admitted that the Donley reference fails to explicitly teach "an active snoop queue (ASQ) module coupled to the request module and configured to maintain a list of requests currently being processed and to prevent simultaneous multiple accesses to a single address in the static portion of the RAM." Without conceding it would have been obvious to have combined Donley and Merchant, to support the Examiner's hypothetical combination, all of the claimed elements, as recited in each claim under rejection, must be disclosed as a result of the proposed combination. As such, for the rejection to be maintained, the Merchant reference must disclose the claimed subject matter.

However, the Merchant reference fails to disclose the "active snoop queue" recited in claims 1 and 10. In the rejection, the Examiner relied upon the snoop queue 408 of the Merchant reference to disclose the recited feature. However, as discussed above, the snoop queue 408, which is part of an external bus logic 406 that is internal to the microprocessor 2, is coupled to the system bus 20 and the external bus controller 410. *See* Merchant, Fig. 4, col. 7, lines 23-31. The snoop queue 408 only accesses the system bus 20. *See id.* Again, the Merchant system is a single system bus configuration and does not disclose multiple processor buses, much less, any device coupled to multiple processor buses. Further, the Merchant reference does not even disclose or suggest a cache coherency module that

comprises the "active snoop queue (ASQ) module." In the Merchant reference, the snoop queue 408 is internal to the microprocessor 2, not part of a cache coherency module coupled to multiple processor buses. As such, the Merchant reference fails to disclose the claimed subject matter. Accordingly, the cited references, either alone or in combination, fail to disclose the claimed subject matter.

Because the cited references, taken alone or in combination, fail to disclose all of the features recited in the instant claims as well as a convincing line of reasoning as to why one of ordinary skill in the art would have found the claimed invention obvious in light of the cited reference, Applicants respectfully assert that independent claims 1 and 10 are patentable over the cited references. Applicants respectfully assert that claims 1 and 10 and the claims dependent thereon are not obvious. Therefore, Applicants respectfully request withdrawal of the rejection and allowance of claims 1 and 10 and the claims depending therefrom.

Second Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 4-6 and 12-14 under 35 U.S.C. § 103(a) as being unpatentable over Donley et al. (U.S Patent No. 5,822,611) in view of Merchant (U.S Patent No. 5,893,151) and McAllister et al. (U.S. Patent Application No. 2003-0200397). Applicants respectfully traverse this rejection.

Claims 4-6 depend from independent claim 1, while claims 12-14 depend from independent claim 10. Based on these dependencies, claims 4-6 and 12-14 are believed to be patentable over the cited references. In the rejection, the Examiner admitted that the Donley and Merchant references do not explicitly teach the specific list structures claimed. In an attempt to cure this deficiency, the Examiner relied upon the McAllister reference to teach the

claimed subject matter. However, the McAllister reference is directed to a memory controller that has separate agents, which are utilized to provide memory transaction coherency. *See* McAllister, page 1, paragraph 2. A directory-based coherency mechanism is utilized to provide coherency between transactions for the system memory controller 22. *See* McAllister, Fig. 1, paragraphs 40 and 41. As such, the McAllister reference does not disclose the recited features discussed above. Therefore, because the McAllister reference does not cure the deficiencies of the Donley and Merchant references, claims 2-4 and 12-14 are patentable by virtue of their dependency on claims 1 and 10. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of claims 4-6 and 12-14.

Third Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 4-7 and 12-15 under 35 U.S.C. § 103(a) as being unpatentable over Donley et al. (U.S Patent No. 5,822,611) in view of Merchant (U.S Patent No. 5,893,151) and VanDoren et al. (U.S. Patent No. 6,279,084). Applicants respectfully traverse this rejection.

In view of the earlier date of invention of the subject matter disclosed and claimed in the present application, Applicants have chosen to remove the VanDoren reference pursuant to 37 C.F.R. § 1.131 and U.S.C. § 103(c). Under Rule 131, Applicants may overcome a prior art rejection by filing an appropriate declaration that establishes the invention of the claimed subject matter for the rejected claims prior to the effective date of the reference. The prior invention may be shown by demonstrating conception of the invention prior to the activity on which the rejection is based coupled with reasonable diligence from prior to the effective date of the reference to the filing of the application.

Here, Applicants have attached a declaration signed by an attorney of record, which demonstrates that the invention disclosed and claimed in the present application was conceived prior to the *issue date* of the VanDoren reference and was reduced to practice with reasonable diligence from prior to the effective date of the VanDoren reference. This Declaration is sufficient to remove the VanDoren reference under 35 U.S.C. § 102(a), thus establishing that the VanDoren reference is only available under 35 U.S.C. § 102(e). Because the VanDoren reference only qualifies as prior art under 35 U.S.C. §§ 102(e)/103, the VanDoren reference is unavailable under 35 U.S.C. § 103(c) with respect to the instant claims, based on the common obligation of assignment, as discussed below.

To utilize the VanDoren reference for an obviousness rejection under 35 U.S.C. § 103, the VanDoren reference must qualify as prior art under 35 U.S.C. § 102, which specifically states:

> A person shall be entitled to a patent unless —
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> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent, or
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> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States, or
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> (c) he has abandoned the invention, or
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> (d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months before the filing of the application in the United States, or
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> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another

> filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language; or
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> (f) he did not himself invent the subject matter sought to be patented, or
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> (g)(1) during the course of an interference conducted under section 135 or section 291, another inventor involved therein establishes, to the extent permitted in section 104, that before such person's invention thereof the invention was made by such other inventor and not abandoned, suppressed, or concealed, or (2) before such person's invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. In determining priority of invention under this subsection, there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

Because the VanDoren reference was filed on October 24, 1997, and issued on August 21, 2001, the VanDoren reference, on its face, only qualifies as prior art against the present application under 35 U.S.C. §§ 102(a) and (e). Sections (b), (c), (d), (f), and (g) of 35 U.S.C. §102 do not apply in the present situation. Under Section (e) of 35 U.S.C. § 102, the VanDoren reference qualifies as prior art. Under Section (a) of 35 U.S.C. § 102, the VanDoren reference facially appears as valid prior art because the VanDoren reference was patented on August 21, 2001, and the present application was filed on September 28, 2001. However, as discussed below, the VanDoren reference does not qualify as prior art under Section (a) because the presently recited subject matter was invented before the issue date of the VanDoren reference.

The conception of the present invention is supported by a letter sent to Mr. Rawlins from Mr. Manware on May 25, 2001. *See* Declaration of Robert A. Manware under 37 C.F.R. § 1.131, herein referenced as "Declaration," paragraph 4. This conception is evidenced by the first draft of the patent application of Exhibit A. As further support of this conception, Mr. Rawlins provided changes to the specification of the patent application on or before June 14, 2001, to Mr. Manware. *See* Declaration, paragraph 5, Exhibit B. In the email, Mr. Rawlins provided specific changes to the first draft of the patent application. As such, this email further supports the conception of the invention at least by May 25, 2001. *See id.* Accordingly, in view of the letter and email exchanged between Mr. Rawlins and Mr. Manware, it is clear that the conception of the claimed subject matter for the rejected claims is prior to the August 21, 2001, which is the issue date of the VanDoren reference.

Furthermore, Applicants provide evidence of reasonable diligence from prior to August 21, 2001, to the filing of the present application on September 28, 2001. The reasonable diligence is supported by: (1) a letter regarding the second draft of the application, which is attached to the Declaration as Exhibit C; (2) a declaration under Rule 63, which is attached to the Declaration as Exhibit D; and (3) an assignment, which is attached to the Declaration as Exhibit E. As noted above, on June 14, 2001, Mr. Rawlins, one of the Applicants, provided changes to the specification of the patent application. *See* Declaration, paragraph 5, Exhibit B. Mr. Manware incorporated the changes into the patent application and forwarded a second draft of the application to the Applicants for review on June 19, 2001. *See* Declaration, paragraph 6, Exhibit C. Once Mr. Manware incorporated the changes from the Applicants, Mr. Manware forwarded a final draft of the above - referenced application, along with a declaration, and assignment

to Applicants. Applicants executed the assignment and declaration on September 28, 2001. *See* Declaration, paragraph 7, Exhibit D and Exhibit E. The present application was then filed on September 28, 2001. As such, Applicants were reasonably diligent from before August 21, 2001, to the filing of the present application on September 28, 2001.

The Rule 131 Declaration establishes that the date of invention of the claimed subject matter is at least as early as May 25, 2001. Thus, the date of invention for the claimed subject matter in the present application is prior to the effective date, i.e., the issue date, of the VanDoren reference under 35 U.S.C. § 102(a). That is, the VanDoren reference is not prior art under 35 U.S.C. § 102(a) because the VanDoren reference issued *after* the date of invention of the present application. As such, the VanDoren reference is only available under 35 U.S.C. §§ 102(e)/103(a).

Because the VanDoren reference is only available under 35 U.S.C. §§ 102(e)/103(a), Applicants may remove the VanDoren reference pursuant to 35 U.S.C. § 103(c). Applicants respectfully refer the Examiner to 35 U.S.C. § 103(c), which states:

> [s]ubject matter developed by another person, which qualifies as prior art under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

In accordance with 35 U.S.C.§ 103(c) and Pub. L. 106-113, § 4807, enacted November 29, 1999, subject matter developed by another person which qualifies as prior art only under subsection (e) of 35 U.S.C.§ 102, shall not preclude patentability where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or

subject to an obligation of assignment to the same person. Here, both the subject matter of the VanDoren reference and the claimed invention were, at the time the invention was made, owned by the same organization or subject to an obligation of assignment to the same organization. The assignee of the VanDoren reference is Compaq Computer Corporation. The assignee of the present application is Compaq Information Technologies Group, L.P. Both of these assignees are wholly owned by Compaq Computer Corporation, which under M.P.E.P 706.02(l)(2) means that they are "commonly owned." Therefore, the VanDoren reference is unavailable as prior art under 35 U.S.C. § 103(c). Furthermore, as the Examiner relied upon the VanDoren reference to disclose subject matter that is not taught in the Donley and Merchant references, the Donley and Merchant references do not disclose or teach all of the claimed subject matter because the VanDoren reference is unavailable. Accordingly, as the rejection of claims 4-7 and 12-15 cannot stand, Applicants respectfully request respectfully request withdrawal of the rejection and reconsideration of the claims.

Conclusion

In view of the remarks set forth above, Applicants respectfully request allowance of the pending claims 1-17. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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